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S2	7120452	signal processing digital word terminal analog period integrated input	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/05/13 12:48

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1 Session 10D: digital and analog test generation: A parametric test method for analog components in integrated mixed-signal circuits

M. Pronath, V. Gloeckel, H. Graeb

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(153.95 KB) Additional Information: full citation, abstract, references

In this paper, we present a novel approach to use test stimuli generated by digital components of a mixed-signal circuit for testing its analog components. A wavelet transform is applied to the response signal of the device under test (DUT). We will show, that in comparison to Fourier transform or no transform at all, particular properties of this transformation are advantageous for mixed-signal test and especially built-in self test.We introduce a new method for test measurement selection based ...

2 Approximate symbolic analysis of large analog integrated circuits

Qicheng Yu, Carl Sechen

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(906.10 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a unified approach to the approximate symbolic analysis of large linearized analog circuits. It combines two new approximation-during-computation strategies with a variation of the classical two-graph tree enumeration method. The first strategy is to generate common trees of the two-graphs, and therefore the product terms in the symbolic network function, in the decreasing order of magnitude. The second approximation strategy is the sensitivity-based simplification of t ...

3 Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn

May 2000 **Proceedings of the 2000 international symposium on Physical design**

Full text available: pdf(247.03 KB) Additional Information: full citation, references

4 From System Specification To Layout: Seamless Top-Down Design Methods for Analog and Mixed-Signal Applications

R. Sommer, I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C.

Clauss, P. Schwarz, G. Noessing
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(462.49 KB) Publisher Site Additional Information: full citation, abstract, citings

Deisgn automation for analog/mixed-signal (A/MS) circuits and systems is still lagging behind compared to what has been reached in the digital area.As System-on-Chip (SoC) designs include analog components in more cases, these analog parts become even more a bottle neck in the overall design process.The paper is dedicated to latest R&D activities within the MEDEA+ project ANASTASIA+.Main focus will be the development of seamless top-down design methods for integrated analog and misx-signal syste ...

5 Behavioral synthesis of field programmable analog array circuits
Haibo Wang, Sarma B. K. Vrudhula
October 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 4

Full text available: pdf(519.64 KB) Additional Information: full citation, abstract, references, index terms

This article presents methods to translate a behavioral-level analog description into a Field Programmable Analog Array (FPAA) implementation. The methods consist of several steps that are referred to as function decomposition, macrocell synthesis, placement and routing, and postplacement simulation. The focus of this article is on the first three steps. The function decomposition step deals with decomposing a high-order system function into a set of lower-order functions. We present an efficien ...

Keywords: Programmable circuits, analog synthesis

6 Session 1D: Analog macromodeling: Simulation-based automatic generation of signomial and posynomial performance models for analog integrated circuit sizing
Walter Daems, Georges Gielen, Willy Sansen
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(163.89 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a method to automatically generate posynomial response surface models for the performance parameters of analog integrated circuits. The posynomial models enable the use of efficient geometric programming techniques for circuit sizing and optimization. To avoid manual derivation of approximate symbolic equations and subsequent casting to posynomial format, techniques from design of experiments and response surface modeling in combination with SPICE simulations are used to gene ...

Keywords: analog circuit modeling, design of experiments, geometric programming, posynomial and signomial response surface modeling

7 Session 5B: Embedded tutorial: CAD solutions and outstanding challenges for mixed-signal and RF IC design: CAD solutions and outstanding challenges for mixed-signal and RFIC design
Domine Leenaerts, Georges Gielen, Rob A. Rutenbar
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(1.87 MB) Additional Information: full citation, abstract, references, index terms

This tutorial paper addresses the problems and solutions that are posed by the design of mixed-signal integrated systems on chip (SoC). These include problems in mixed-signal

design methodologies and flows, problems in analog design productivity, as well as open problems in analog, mixed-signal and RF design, modeling and verification tools. The tutorial explains the problems that are posed by these mixed-signal/RF SoC designs, describes the solutions and their underlying methods that exist toda ...

8 A two-layer library-based approach to synthesis of analog systems from VHDL-AMS specifications

Alex Doboli, Nagu Dhanwada, Adrian Nunez-Aldana, Ranga Vemuri

April 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 2

Full text available: pdf(658.00 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a synthesis methodology for analog systems described using VHDL-AMS language. Synthesis produces net-lists of analog components that are selected from a library, and sized so that specified objectives (like AC response, signal to noise ratio, dynamic range, area) are optimized. The gap between abstract specifications and implementations is bridged using a two-layered methodology. The first layer is architecture generation. The second layer is component synthesis and constrain ...

Keywords: Analog synthesis, VHDL-AMS, branch-and-bound, genetic algorithms, performance estimation

9 Synthesis tools for mixed-signal ICs: progress on frontend and backend strategies

L. Richard Carley, Georges G. E. Gielen, Rob A. Rutenbar, Willy M. C. Sansen

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(91.08 KB) Additional Information: full citation, references, citings, index terms

10 Low-power analog design: A fully integrated physical activity sensing circuit for implantable pacemakers

Alfredo Arnaud, Carlos Galup-Montoro

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(395.61 KB) Additional Information: full citation, abstract, references, index terms

This paper shows the implementation of a fully integrated Gm-C 0.5-7Hz bandpass filter-amplifier with gain G=400, for a piezoelectric accelerometer which is part of a rate adaptive pacemaker. The fabricated circuit operates up to 2V power supply, consumes only 230nA current, and achives 2.1uVrms input noise. Detailed circuit specifications, measurements, and a comparative analysis of the system performance are presented.

Keywords: CMOS, analog design, biomedical, low-power

11 Metrics, techniques and recent developments in mixed-signal testing

Gordon W. Roberts

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(240.28 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This paper presents a tutorial on mixed-signal testing. Our focus is on testing the analog portion of the mixed-signal device, as the digital portion is handled in the usual way. We begin by first outlining the role of test in a manufacturing environment, and its impact on

product cost and quality. We look at the impact of manufacturing defects on the behavior of digital and analog circuits. Subsequently, we argue that analog circuits require very different test methods than those presently used ...

Keywords: manufacturing defects, manufacturing environment, measurement setups, mixed analogue-digital integrated circuits, mixed-signal testing, product cost, quality

12 On-chip analog output response compaction
M. Renovell, F. Azais, Y. Bertrand
March 1997 **Proceedings of the 1997 European conference on Design and Test**

Full text available: pdf(633.96 KB) Publisher Site Additional Information: full citation, abstract, citings

In this paper, we propose a technique for on-chip analog output response compaction in order to implement self-test capabilities in analog and mixed-signal integrated circuits. The integration function is identified as a powerful analog compression scheme and an analog signature analyzer is proposed. The op amp-based implementation allows one to define single and multiple-input versions. The multiple-input analyzer permits the monitoring of some extra internal nodes in addition to the classical ...

Keywords: analog compression scheme, analog output response compaction, analog signature analyzer, automatic testing, circuit testability, concurrent control, fault coverage, integration function, internal nodes, mixed-signal integrated circuits, multiple-input version, on-chip response evaluation, op amp-based implementation, self-test capabilities, single-input version

13 A Method for Parameter Extraction of Analog Sine-Wave Signals for Mixed-Signal Built-In-Self-Test Applications
Diego Vázquez, Gildas Leger, Gloria Huertas, Adoración Rueda, José L. Huertas
February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Full text available: pdf(127.60 KB) Additional Information: full citation, abstract, index terms

This paper presents a method for extracting, in the digital domain, the main characteristic parameters of an analog sine-wave signal. The required circuitry for on-chip implementation is very simple and robust, which makes the present approach very suitable for BIST applications. Solutions in this sense are addressed together with simulation results that validate the feasibility of the proposed approach.

14 Interpretable symbolic small-signal characterization of large analog circuits using determinant decision diagrams
Xiang-Dong Tan, C.-J. Richard Shi
January 1999 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(161.78 KB) Additional Information: full citation, index terms

15 Wireless telecom silicon integration: analog design for radio, baseband and speech spectrum
J. Sevenhans, D. Haspeslagh, J. Wenin
January 1998 **Wireless Networks**, Volume 4 Issue 1

Full text available: pdf(324.74 KB) Additional Information: full citation, abstract, references, citings, index terms

The application today, pushing analog design for CMOS and RF-bipolar into new frontiers is definitely the mobile radio telephony. New telecom systems like GSM, PCN, DECT, DCS, Wireless in the loop...are all developing very rapidly and will enable us very soon to organise a complete telephone network with full coverage for your car, as well as in your kitchen and on your office desk. In Europe the major telecom companies have worked together to establish one common standard for cellular mobi ...

16 Low Cost Analog Testing of RF Signal Paths
Marcelo Negreiros, Luigi Carro, Altamiro A. Susin
February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**
Full text available: pdf(374.70 KB) Additional Information: full citation, abstract, citings, index terms

A low cost method for testing analog RF signal paths suitable for BIST implementation in a SoC environment is described. The method is based on the use of a simple and low-cost one-bit digitizer that enables the reuse of processor and memory resources available in the SoC, while incurring little analog area overhead. The proposed method also allows a constant load to be observed by the circuit, since no switches or muxes are needed for digitizing specific test points. Mathematical background and ...

17 Circuit complexity reduction for symbolic analysis of analog integrated circuits
Walter Daems, Georges Gielen, Willy Sansen
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(144.40 KB) Additional Information: full citation, references, index terms

18 Dynamic test signal design for analog ICs
Giri Devarayanadurg, Mani Soma
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(149.26 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper we present an approach to construct dynamic test signals for analog circuits. Using the integral measure for characterizing time-domain signals, we extend the minmax formulation of the static test problem to the dynamic case. A sub-optimal solution strategy, similar to dynamic programming methods is used to construct the test waveforms. The approach presented here may be used to construct input signals for an on-chip test scheme or for the selection of an external stimulus applied ...

Keywords: analog, test, dynamic, time-domain, optimization, minmax

19 Analog design: Modeling and designing high performance analog reconfigurable circuits
Eric E. Fabris, Luigi Carro, Sergio Bampi
September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**
Full text available: pdf(272.91 KB) Additional Information: full citation, abstract, references, index terms

The theoretical model for a mixed signal front-end interface for the SOC employing a fixed analog cell is presented in this work. The set of developed equations can be used for high level design space exploration. Moreover, the proposed architecture leads to programmable analog processing functions using digital modules, well suited to current FPGAs platforms and general purpose SOC. Some guidelines are addressed on how the proposed architecture

can lead to greater level of analog design automat ...

Keywords: FPAA, analog design, analog programmability, band-pass sigma-delta modulator

20 Behavioral synthesis of analog systems using two-layered design space exploration

Alex Doboli, Adrian Nunez-Aldana, Nagu Dhanwada, Sree Ganesan, Ranga Vemuri

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

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